Silanna Semiconductor | Power Management Re-Imagined

SZPL3002A

65W DCDC with Integrated USB-PD PORT IC

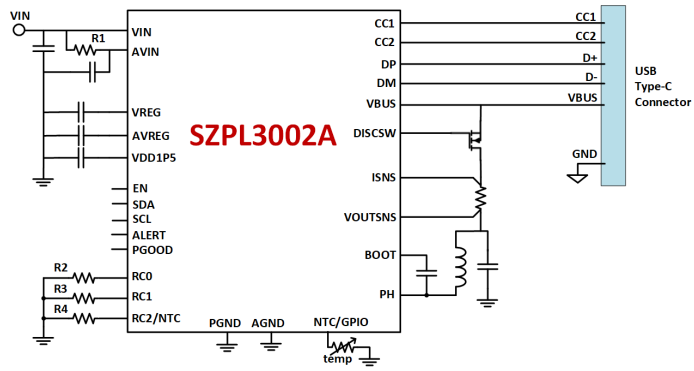
Features

- Synchronous buck regulator with Switching Frequencies up to 2 MHz
- Integrated USB-PD Controller supporting USB-PD R3.0, PPS, BC1.2, QC 2.0/3.0/4.0/4.0+/5.0 Support
- Intelligent Multiport Power Sharing and Power Re-balancing
- High Efficiencies (>98%)
- Selectable Power Saving Mode
- Selectable Power Contract Configurations – reduces required programming
- Temperature Triggered Power Throttling
- VCONN power generation for e-Marked Cables
- Wide Input Voltage Range: 7.0 V to 27 V
- Supports Vout of 3.3 ~ 21.5 V, at 3.25 A
- UVLO/OCP/OVP/UVP/OTP Protections
- QFN 5 mm x 5 mm Thermally Enhanced Package
- Configurable as either a Type-C or a Type-A port

Applications

- AC/DC Chargers with USB-PD Support
- Multiple Output USB-PD Charging Strips
- USB-PD Outputs in Displays and TVs
- Docking Stations and Laptops

Application Diagram



Product Description

The SZPL3002A is a high efficiency, synchronous buck converter along with a USB-PD controller creating a complete, single IC, downstream facing USB-PD compliant port. The device can supply fixed output voltages as well as Programmable Power Supply (PPS) profiles for fast charging to connected devices.

The device also supports the Qualcomm® QuickCharge™ protocols, QC2.0/3.0/4.0/4.0+/5.0, supporting Type-C output ports as well as Type-A ports.

A 100 mW VCONN power supply is included for powering and reading e-marked cables.

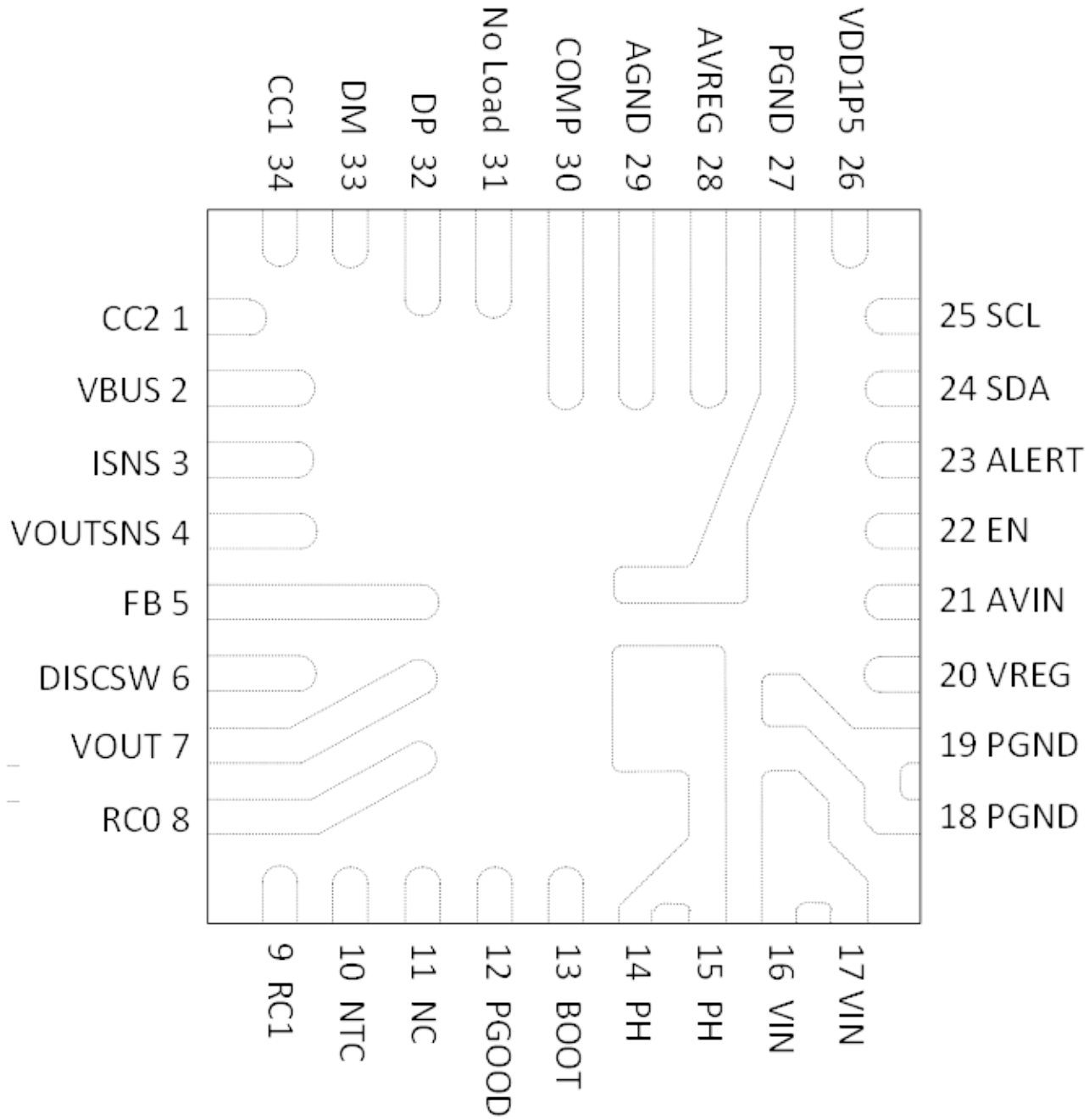
An I²C bus is present to communicate with the internal PD-Controller for advanced applications in Intelligent Power Sharing for multiple output charging ports. It automatically re-balances the power between ports as demand continuously changing

It is capable of Power Derating during over temperature events. This is a programmable setting through one time configuration registers.

The buck converter is optimized for the highest efficiency performance across the output voltage range of 3.3 V to 21.5 V.

The SZPL3002A is available in a compact QFN 5 mm x 5 mm package to deliver the best power and function density with a minimum external component count.

Package Pinout

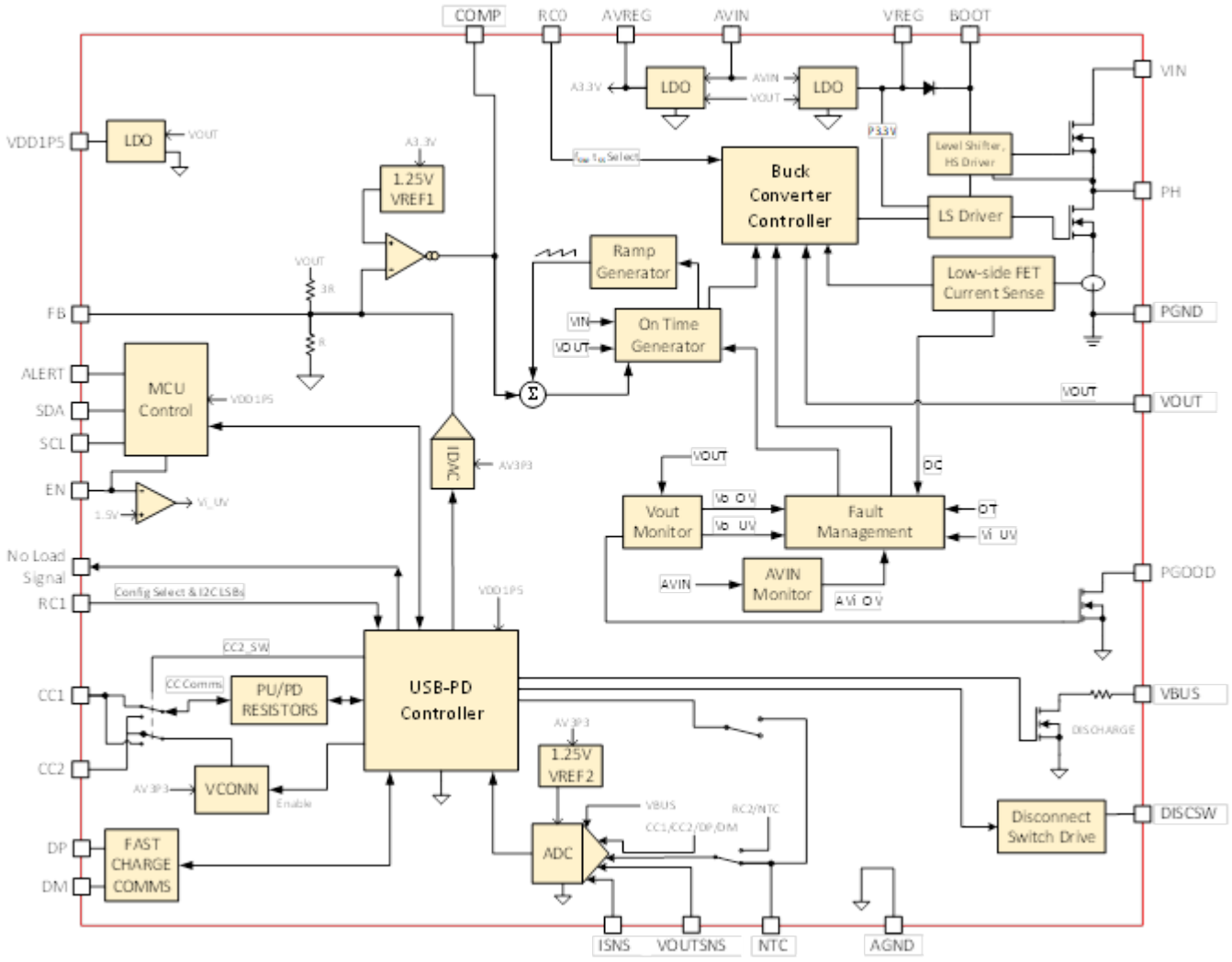


Package Pinout - Top View

Pin Definitions

Pin #	Name	Description
1	CC2	Configuration Channel for USB-PD communications or VCONN supply output. Must be connected to DM for A Port configuration
2	VBUS	Discharge FET output and VBUS voltage sense line. Connect to VBUS through a load resistor.
3	ISNS	High side current sense, analog input. Uses a 5 mΩ series resistor inserted between VOUT and the VBUS disconnect switch. Connect this pin to the disconnect switch side of the current sense resistor.
4	VOUTSNS	VOUT sense line and high side output current sense analog input. Connect this pin to the VOUT side of the output current sense resistor.
5	FB	PD controller manages the output voltage. This pin should **only** be used for compensation purposes and no DC load on this pin.
6	DISCSW	Gate drive signal for N-channel disconnect switch.
7	VOUT	VOUT power input to internal LDO circuitry. Connect this pin anywhere along the VOUT signal path.
8	RC0	Analog input, a resistor to ground sets conversion frequency (F_{SW}) and soft start time (t_{SS}) .
9	RC1	Analog input, resistor to ground selects the USB PD contract configuration set and I2C device address.
10	NTC	Connect an NTC resistor to ground.
11	NC	Connect to GND.
12	PGOOD	Power good output signal. Active high, open drain output. Connect to a pullup resistor to VREG.
13	BOOT	Bootstrapped supply decoupling. Floating supply to the high side driver of the buck converter. Connect to 0.1 uF capacitor to the PH node.
14, 15	PH	Phase (switch) node of buck converter output. Connect to output inductor.
16, 17	VIN	Supply input to buck converter. Decouple locally as per datasheet guidance.
18, 19	PGND	Power ground of the buck converter. Connect to ground plane through shortest available path.
20	VREG	Output of internal linear regulator for buck converter gate driver supply. Connect to a 1 uF bypass capacitor to ground.
21	AVIN	Supply input to buck converter's internal LDOs.
22	EN	Analog control input. A potential higher than the UVLO threshold enables switching operation and output soft start process. A potential lower than the shutdown threshold places the device in a low power state. Decouple with one 1 nF to 100 nF capacitor placed close to the part. See the application information section for a more detailed explanation of operation.
23	ALERT#	Open drain output, active low. Asserted low by slave device during power sharing operation.
24	SDA	Bi-directional data line for I2C communications
25	SCL	Clock line input for I2C communications
26	VDD1P5	1.5 V regulator output. Connect to a 1 uF bypass capacitor to ground.
27	GND	Ground connection.
28	AVREG	Analog circuits, buck converter, 3.3 V regulator output. Connect to a 1 uF bypass capacitor to ground.
29	AGND	Analog ground.
30	COMP	Buck converter loop compensation node, series RC to ground. See the applications section for additional information.
31	No Load	No Load indicator pin. Pulled high at no load
32	DP	USB Data Plus signal for proprietary fast charging communication.
33	DM	USB Data Minus signal for proprietary fast charging communication.
34	CC1	Configuration Channel for USB-PD communications or VCONN supply output. Must be connected to DP for A Port Configuration.

Internal Block Diagram



Internal Block Diagram

Absolute Maximum Ratings

(Ta = 25°C Unless Otherwise Specified.) (1)

Parameter	Symbol	Conditions	Min.	Max.	Units
Input Supply Voltage (DC)	V_{AVIN}, V_{VIN}	Relative to PGND	-0.3	28	V
V_{PH} (AC, <10ns)	V_{PH}	Relative to PGND	-2	35	
Digital I/O Pins	V_{SDA}, V_{SCL}, V_{EN}, V_{PGOOD}, V_{ALERT}	Relative to AGND	-0.3	6	
Digital Communication Pins	V_{CC1}, V_{CC2}, V_{DP}, V_{DM}	Relative to AGND	-0.3	AVIN	
Storage Temperature Range	T_{STG}		-50	150	°C
Operating Junction Temperature	T_J		-40	125	
Electrostatic Discharge Rating (2) (3)	V_{ESD}	HBM, Human Body Model per ANSI/ESDA/JEDEC JS-001, all pins	-2000	2000	V

Notes:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
3. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

See Notes 1 and 2.

Parameter	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	$R_{\Theta JA}$		30.1		°C/W
Thermal Resistance Junction to Top of Package	$R_{\Theta JC(TOP)}$		13.7		
Thermal Resistance Junction to Board	$R_{\Theta JB}$		7.5		
Thermal Characterization Parameter - Junction to top case	Ψ_{JT-TOP}		1.4		
Thermal Characterization Parameter - Junction to bottom case	Ψ_{JB-BOT}		3.0		
Thermal Characterization Parameter - Junction to board	Ψ_{JB-BOT}		7.5		

Notes:
Using a 4-layer (FR4, 2S2P) JEDEC board with four thermal vias as per specification JESD51-5.
Based upon simulations.

Recommended Operating Conditions

(Ta = 25°C Unless Otherwise Specified.) (1)

Parameter	Symbol	Conditions	Min.	Max.	Units
Power Stage Input Supply Voltage (2)	V_{AVIN}, V_{VIN}	Relative to PGND	8	27	V
Output Currents	I_{OUT-DC}	DC, Continuous		3.25	A
Operating Junction Temperature			-40	125	°C

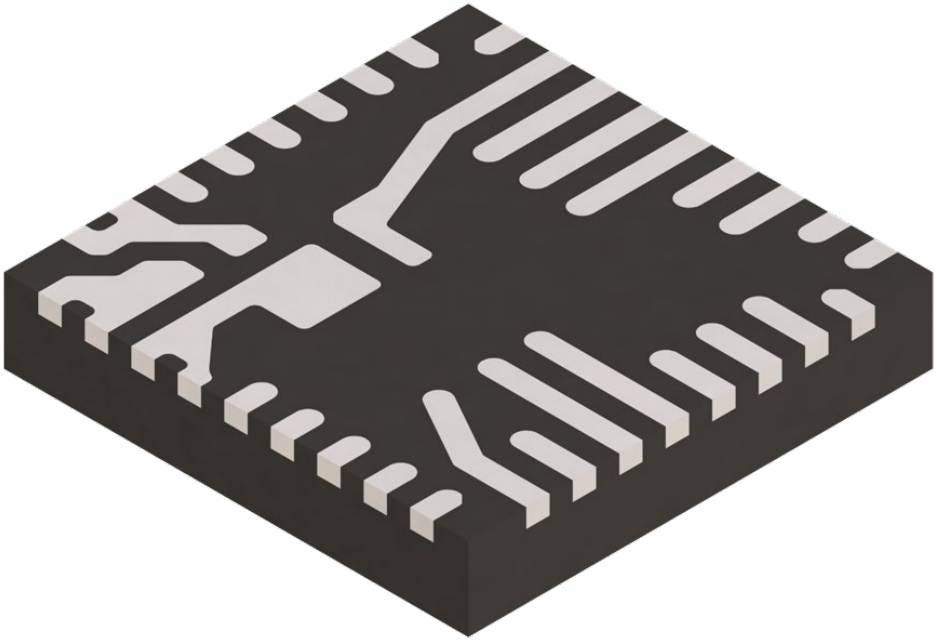
Notes:

1) Device functionality is not guaranteed outside the recommended operating conditions.
2) Attention to proper VIN and AVIN input supply bypassing and tight PCB layout must be observed to keep the peak voltage of any ringing on the phase node, at the PH pins, below the Absolute Maximum Ratings above.
3) The actual operating temperature will depend on the thermal foldback setting which is lower than this max limit

Product Ordering Information

Part Number	Feature
SZPL3002A-00-AF55	Integrated USB-PD Port IC; unprogrammed

Product Image



SZPL3002A Product Image

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Revision History

Revision	Date	Author	Note
1.0	08/07/2022	HN	Preliminary Release.
2.0	02/28/2023	HN	Update pin naming
3.0	07/11/2023	HN	Remove “preliminary”, update electrical table and final release to document control

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